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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,538	11/07/2001	Luca Battu'	851763.420	2722

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EXAMINER	
PATEL, SHAMBHAVI K	
ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 08/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,538	BATTU' ET AL.	
	Examiner	Art Unit	
	Shambhavi Patel	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/22/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Request for Continued Examination filed on 17 July 2006. Claims 1-23 have been presented for examination.

Priority

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Europe on 11/07/2000. It is noted, however, that the Examiner is unable to locate a certified copy of the 00830735.7 application as required by 35 U.S.C. 119(b). At this time, the Examiner is requesting a replacement certified copy of the priority document.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 22 March 2002 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner has considered the IDS as to the merits.

Claim Interpretation

Regarding claims 1, 10, and 13, the *phrase 'emulated at hardware level' is interpreted in light of* ***page 4*** *of the specifications,* which states that the system may be configured in the form of a general-purpose digital computer which, appropriately programmed, implements the above-mentioned process. The prior art teaches simulating the circuit at gate-level or RT-level *(analogous to hardware level)* using software that runs on a computer **(abstract; sections 3 and 4)**.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

1. **Claims 1-4, and 6-12 are rejected under 35 U.S.C. 101** because the claimed invention is directed to non-statutory subject matter. The Examiner asserts that the current state of the claim language is such that a reasonable interpretation of the claims would not result in any useful, concrete or tangible product. *Merely determining a value indicative of the number of transitions in a circuit does not produce a tangible result.*

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. **Claim 1-23 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Jochens et al. ('Application of Toggle-Based Power Estimation to Module Characterization' February 1997),** herein referred to as Jochens.

Regarding claims 1, 10, and 13:

Jochens is directed to a process, system, and apparatus **(sections 3 and 4)** for estimating power consumption, over a given time interval **(abstract)**, of a digital circuit described at a hardware level using a functional element provided with input/output terminals **('Introduction'**

paragraph 2), the process comprising estimating the power consumption based on the number of transitions performed by the functional element during said time interval **('Introduction' paragraph 3)** including

a. emulating at hardware level the digital circuit **('Introduction' paragraph 2**, using additional elements associated to and coupled to said functional element at said hardware level **('Introduction' paragraph 3)**, said additional element being able to detect, during emulation of the digital circuit, at least one signal indicative of a behavior, and hence of power consumption of the associated functional element during said time interval **('Introduction' paragraph 4).** The *toggle count mechanism employed by the prior art is analogous to attaching an additional element to output of the functional element*, because it is able to detect switching activity at the output terminal of the functional gate **(equations 2-3 and accompanying descriptions).**

b. acquiring a value of said at least one signal during the emulation of the digital circuit **(equation 3)**, said value being indicative of the number of transitions **(equation 3 value N(T))** and usable to determine the power consumption of said associated functional element is said given time interval **('Concept of Simulation' paragraph 5)**

Regarding claim 2:

Jochens is directed to the process according to claim 1, wherein emulating said digital circuit using said additional elements associated to and coupled to said functional element

includes coupling said additional elements to an output of the functional element **('Concept of Simulation' paragraph 4)**. The toggle count mechanism *(analogous to the additional element)* functions by associating itself with the output of the gate in order to measure the switching activity.

Regarding claims 3, 11 and 14:

Jochens is directed to the process according to claim 1 wherein said additional elements are able to obtain, during said given time interval and during said emulation of the digital circuit: a count of said transitions to obtain said number of transitions **('Concept of Simulation' paragraph 4; equation 3 value N(T))**

a. A fraction of time in which a state of the associated functional element is stable **(equations 2-3)**. The toggle mechanism tracks how many transitions are made during the time interval, and can thus calculate how many times the signal was at a high or low. This data can also be found in the VCD file created by the simulator.

b. The value of said number of transitions and said fraction of time being indicative of the power consumption of said functional element during said time interval **('Concept of Simulation' paragraph 4)**

Regarding claim 4:

Jochens is directed to the process according claim 1, further comprising controlling acquisition of the value of said at least one signal using hardware events monitored by logic

analyzers active on the additional elements **('Concept of Simulation' paragraph 4).** The toggle count mechanism *(analogous to the additional element)* functions by associating itself with the output of the gate, and monitors the output signal in order to track transitions.

Regarding claim 5:

Jochens is directed to the process according to claim 1, further comprising accessing information stored in said additional elements and storing said information in view of subsequent processing **(figure 1; 'Concept of Simulation' paragraph 5)**

Regarding claim 6:

Jochens is directed to a processing system configured to implement the process according to claim 1 **(sections 3 and 4).** The power estimation tool disclosed in the prior art is tested on various circuits.

Regarding claim 7:

Jochens is directed to a computer program product directly loadable into an internal memory of a digital computer, comprising software code portions to perform the process of claim 1 when said program is run on the computer **(sections 3 and 4).** The power estimation tool disclosed in the prior art is tested on various circuits. In order for this to be done, the tool must be loaded onto the computer.

Regarding claims 8, 9, 12, and 16:

Jochens is directed to the process of claim 1 wherein emulating at the hardware level includes emulating at a register transfer level or gate level **('Concept of Simulation' paragraph 8)**.

Regarding claim 15:

Jochens is directed to the apparatus of claim 13 wherein the third module includes machine-readable instructions stored on a machine-readable medium and executable by a processor **(abstract).** The simulators are all usable by a computer to model and simulate the circuit design **(as shown in sections 3 and 4)**

Regarding claims 17, 20, and 22:

Jochens is directed to coupling said additional element to said functional element at said hardware level, wherein this modifies the digital circuit by forming part of said digital circuit at said hardware level, without modification of an original functionality of said digital circuit **('Introduction' paragraphs 3-5; 'Concept of Simulation' paragraphs 6-7).** The toggle power mechanism works by associating itself with the output of the functional element. This is functionally equivalent to inserting itself into the hardware description, because by tying itself to the output pin, it can count the number of transitions on the signal.

Regarding claims 18, 19, 21, and 23:

Jochens is directed to using said additional elements to detect the number of transitions during operation of the digital circuit in real time **(('Concept of Simulation' paragraphs 4-5; equation 3 number of transitions N(T)))**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is (571) 272-5877. The examiner can normally be reached on Monday-Friday, 8:00 am – 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

08/17/2006

KAMINI SHAH
SUPERVISORY PATENT EXAMINER